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Introduction

 10 bits of vertical resolution per channel and either 1.25 Gigasamples per second (GS/s) or 625 Megasample per second (MS/s) rate provides wideband waveforms with exceptionally low EVM

- Dual output channels drive both single-ended and balanced designs without the need for baluns or hybrids
- Extended memory and advanced sequencing engine allows for extended simulations of complex waveform propagation models
- Multiple module synchronization provides multi-emitter simulations suitable for MIMO applications
- Multiple programmatic interfaces enable easy integration into existing test environments
- Fully compliant to LXI Class A standards

Generate Wide Bandwidth AND Low EVM Signals, Simultaneously

The Keysight Technologies, Inc. N8242A is a wideband arbitrary waveform generator (AWG) capable of creating digitally modulated waveforms for wideband communication systems. Each channel of the N8242A operates at either 1.25 GS/s sample rate (option 125) or 625 MS/s sample rate (option 062) and features 10 bits of vertical resolution, which is ideal for compliance testing of digital radios targeted for use with emerging communication standards such as MB-OFDM ultra wideband, 802.11n, MIMO, and proprietary wideband formats. This LXI synthetic instrument module offers dual differential output channels to drive both single-ended and balanced designs. The AWG also supports advanced sequencing and triggering modes to create eventbased signal simulations. Multiple N8242A modules can be synchronized for the generation of phasecoherent, multi-emitter scenarios. Waveform development tasks are simplified using the AWG's numerous programmatic interfaces including complete instrument control from the MATLAB command line. When the N8242A is combined with a wideband I/Q upconverter, modulation bandwidths of 1 GHz can be realized at RF frequencies for signal simulations employed in functional testing of chip sets designed for modern digital communications radios.¹



Figure 1a. Generate MB-OFDM compliant UWB waveforms.

Extended performance

The N8242A gives designers access to Digital-to-Analog Converter (DAC) technology capable of generating wideband digital communications signals with ultra-low EVM. Each module incorporates two high-speed DACs to create 500 MHz of signal bandwidth and \leq -50 dBc SFDR across each channel. Users have the choice of driving their designs differentially from the DAC outputs or through multiple signal-conditioning paths. Although some AWGs require users to make a trade-off between the number of output channels and differential outputs, the N8242A provides both—allowing you to drive your designs and eliminating the need for baluns or hybrids in the test path. In addition, each channel can output waveforms as an IF or as a baseband signal for I/Q upconversion.



Figure 1b. Create UWB reference waveforms with low EVM.

1. Keysight E8267D PSG signal generator with option 016 wideband I/Q inputs.



Sequence repeat

Figure 2. Create sophisticated signal scenarios by looping and nesting waveforms.

Create long scenario simulations

Multiply the effective size of onboard memory through the use of the N8242A's advanced sequencing engine. Uniquely define how waveform segments are played through looping and nesting of stored waveform models. This capability gives users the ability to simulate fading and other multi-path effects for extended periods of time.



Figure 3. Multi-path effects can be simulated through propagation models.

System scalability

Create phase-coherent, multi-emitter simulations using the N8242A's precision SYNC clock. A single N8242A can drive a total of eight AWG modules to synchronize their outputs on a sample-by-sample basis. Any number of modules can be synchronized with simple driver hardware. The AWG also includes multiple front-panel trigger and markers for complete system synchronization.

Ease-of-use

The N8242A's graphical user interface guides developers through module setup and waveform file transfers. Users can quickly configure the instrument's signal conditioning paths, marker and trigger lines, sample and reference clock sources and simple sequencing functions. More sophisticated sequencing functions are available through the instrument's numerous programmatic interfaces. The N8242A supports interfaces for MATLAB, LabView, IVI-C, and VEE framework.

Figure 4. The N8242A's compact LXI modular size is perfect for integrating into ATE system racks.

Luck Hay Luck Hay Channel I Wavelone Durned 2 Wavelone Durned (M) 0500	Channel 1 Waveform:	CHI
Rey Mode: Ottee MM [0.00] → © Continuous Ottee MM [0.00] → Batt Count Ottee MM [0.00] → Address: TCPF=Lang2A1a 90501; invi0.3NSTR Soud MI [0.50] → Souder → Swidtl: User MM [0.00] → Output (M) [0.50] → Advect TCPF=Lang2A1a 90501; invi0.3NSTR PV Ventor: Advect TCPF=Lang2A1a 90501; invi0.3NSTR Souder → Count (M) [0.50] → PV Ventor: Advect TCPF=Lang2A1a 90501; invi0.3NSTR Souder → Count (M) [0.50] →	Channel 2 Markers:	
Instrument Info Address: TCFIP:-an8241a-9001:inr0.INSTR Soud BL 9500001 PW Versine A300 Output (M) [050] -2 Active Amp Other (M) [050] -2	Tay Mode: Continuous Burst Count Start	Office (V); 0.000 😒
	istunient Irlo Addees: TCPIP::a-e8241a-90501:inst0.:INSTR Said #L US4039001 PW Vanion: A300	Durput (Y) (050)

Figure 5. Directly import and play waveforms from the Quick Play menu.

Figure 6. Play waveforms files directly from the MATLAB command line.

New! Enhanced Capabilities for the N8242

Dynamic Sequencing (option 300)

The dynamic sequencing software enables radar and military communications engineers to build custom signal scenarios on the fly. Engineers can dynamically access up to 16 k of previously stored sequences through a 16-bit interface and replay these complex waveforms to respond to changing threat environments, or to create signals where the next waveform to be played is not known in advance.

Direct Digital Synthesis (option 330)

The direct digital synthesis (DDS) enables radar and emerging-communications engineers to create basic waveforms in the AWG's memory and then modify their behavior with profiles for amplitude modulation, phase modulation and frequency modulation. This enables engineers to simulate testing without the time and expense of field trials, such as in-flight and in-orbit testing.

This option can also be used to simulate fading profiles in receiver testing for satellite and 4G signals, such as multiple input, multiple output formats (MIMO).

Figure 7. Create signals where the next waveform to be played is not known in advance.

Figure 8. Define signals by carrier frequency and modulation-instant by instant.

Key Characteristics

Channels	Two independent channels available as baseband CH1: Single-ended and differential CH2: Single-ended and differential	or IF outputs
Modulation bandwidth	1.25 GS/s sample rate (option 125) 500 MHz per channel (1 GHz IQ bandwidth)	625 MS/s sample rate (option 062) 250 MHz per channel (500 MHz IQ bandwidth)
Resolution	10 bits (1/1024 levels)	
Output spectral purity – (CH1 and CH2)	 1.25 GS/s sample rate (option 125) Harmonic distortion: ≤ -50 dBc for each channel DC to 500 MHz Non-Harmonic spurious: ≤ -75 dBc for each channel 1 kHz to 500 MHz Noise floor: ≤ -150 dBc/Hz across the channel bandwidth 	625 MS/s sample rate (option 062) Harmonic distortion: ≤ -50 dBc for each channel DC to 250 MHz Non-Harmonic spurious: ≤ -75 dBc for each channel 1 kHz to 250 MHz Noise floor: ≤ -150 dBc/Hz across the channel bandwidth

Figure 9. Excellent harmonic and spurious performance are available across the full bandwidth of each channel.

Figure 10. Spurious performance outstanding at low signal frequencies.

Sample clock	
Internal	Fixed 1.25 GS/s (option 125)
	Fixed 625 MS/s (option 062)
Internal clock output	+3 dBm nominal
External clock input	Tunable 100 MS/s to 1.25 GS/s (option 125)
	Tunable 100 MS/s to 625 MS/s (option 062)
External clock input drive level	+5 to –15 dBm typical
Phase noise characteristics	1 kHz: –95 dBc/Hz
	10 kHz: –115 dBc/Hz
	100 kHz: -138 dBc/Hz
	1 MHz: –150 dBc/Hz
Noise floor	–150 dBc/Hz
Accuracy	Same as 10 MHz timebase input
Frequency reference Input drive level	+2 to +12 dBm into 50 Ω (+2 dBm nominal)
Waveform length	8 MS per channel (16 MS with option 016)
Minimum waveform length	128 samples
Waveform granularity	8 samples
Segments	1 to 32 k unique segments can be defined consisting of waveform start and stop address,
	repetitions and marker enable flags.
Segment loops	A total of 1 million (2 ²⁰) loops can be defined for each segment. Loops can be configured to
	advance in one of four modes:
	 Single: The segment loop plays once and waits at the end of the loop for a trigger.
	- Continuous: Segment loop is repeated continuously until a trigger is received.
	 Auto: Automatically advances to the next segment after completing the specified number of loop
	repeutions. Papaget: The waveform loop repeate until the number of waveform loop repetitions is mot
Sequences	Up to 32 k total unique waveform sequences can be defined. A sequence is a contiguous
	Series of waveform segments.
Advanced sequencing	Enables users to build and playback scenarios, which are comprised of one of more
	sequences.
Scenarios	1 to 16 k pointers can be assigned to play pre-defined sequences. Sequence play begins with
	the first sequence entry and continues uninterrupted until the last entry is played. The table
	repeats until stopped.

Scenario jump modes	Scenario jumps determine how a sequence responds to a jump trigger. There are no disconti- nuities in a scenario jump other than those imposed by the waveform data. Three modes are
	available to control scenario jumps: lump immediate: .lumps immediately to the next specified scenario address with a fixed latency
	 End of waveform: The current waveform (including repeats) is completed before jumping to a new

- scenario.
- End of scenario: The current scenario is completed before jumping to a new scenario. Jump latency is the longer of either the jump immediate latency or the length of the remaining scenario.

Additive White Gaussian Noise (option 2	50)
Noise pedestal bandwidth	500 MHz
Crest factor	15 dB
Noise amplitude accuracy	±0.5 dB
Dynamic Sequencing (option 300)	
Input	20-pin mini-D connector
Input levels	All pins configured as 2.5 volt LVCMOS inputs. A logic low must fall within the -0.2 to +0.5 volts window. A logic high must be within the window of +2.0 to +2.8 volts.
Number of address bits	13 bits per channel
Total number of addressable scenarios	16 k
Data rate for dynamic data	100 ns
Data latency	Same as front panel trigger inputs. Software pointers may also be used to point to pre-defined scenarios, though latencies are not deterministic.
Direct Digital Synthesis (option 330)	
Output frequency resolution	1 Hz
Frequency modulation	Deviation from 0 to 125 MHz (250 MHz peak-peak)
Phase modulation	Deviation from -180 to +180 degrees in 0.022 degree steps
Amplitude modulation	Modulation depth from 0 to 100% with 15 bit resolution
Single channel bandwidth	400 MHz (800 MHz I/Q)

External triggers			
Number of inputs	8 each (4 SMB female front-panel connectors plus four software triggers over the		
	LXI interface from host processor)		
Trigger polarity	Negative/positive		
Trigger impedance	2 k Ω		
Maximum input level	±4.5 volts		
Input sensitivity	250 mV		
Trigger threshold	-4.3 volts to +4.3 volts		
Trigger timing resolution	Sample clock/8	Sample clock/8	
	(6.4 ns at 1.25 GS/s rate) (option 125)	(12.8 ns at 625 MS/s rate) (option 062)	
Trigger latency	34 times clock/8	34 times clock/8	
	(217.6 ns at 1.25 GS/s rate) (option 125)	(435.2 ns at 625 MS/s (option 062) rate)	
Trigger uncertainty	< 50 ps		
Minimum trigger width	12.8 ns at 1.25 GS/s clock rate (option 125)	25.6 ns at 625 MS/s clock rate (option 062)	
Trigger delay	Programmable from 1 to 256 sync clock cycles	with 1 sync clock cycle resolution ²	
LXI triggering modes			
Driver command based	A driver interface on the controlling computer is used to directly transmit a command to the		
	module.		
Direct LAN messaging	A data packet containing triggering information (including a time stamp) is sent directly from one		
	module to another via the LAN.		
Time based events	An IEEE 1588-based time trigger is set and executed internally in a module.		
LXI trigger bus-based	A module function is triggered via a voltage on the LXI trigger bus.		
The LXI triggering conforms to the			
specifications of the LXI standard,			
revision 1.0,			

2. A sync clock cycle is clock/8

External markers			
Markers	Can be defined for ea	ch waveform segment.	
Number of outputs	4 each SMB female		
Marker polarity	Negative, positive		
Output impedance	50 Ω		
Marker low level	100 mV nominal into	high impedance load	
Marker high level	3.2 volts nominal into high impedance load		
Marker timing resolution	Clock/8 (6.4 ns at 1.25 GS/s r	ate) (option 125)	Clock/8) (12.8 ns at 625 MS/s rate (option 062)
Marker latency	Marker precedes analog output and is adjustable in 2 sample clock period steps.		
Marker latency repeatability	<100 ps		
Marker width	Programmable from ²	1 to 256 sync clock cycles ² , witl	n 1 sync clock cycle resolution
Marker delay	Programmable from -	-8 to 502 sample clock cycles,	with 2 sample clock cycle resolution
LXI markers	Two LXI markers are	available	
Module synchronization	Supports system sca a fan-out of 8 N8242, used to scale any nur	ling for any number of N8242A I A modules for precise triggering nber of modules.	modules. A single module can support g and repeatability. Driver boards may be
Sync clock output level	800 mV p-p (50 Ω , A	C coupled)	
Sync clock input sensitivity	100 mV p-p minimum	into 50 ${f \Omega}$ AC coupled	
Analog output			
Output connector	SMA female		
Output impedance	50 Ω		
Analog output levels	The following output	levels are specified into 50 Ω	
		Single-ended	Differential
	Passive mode	0.5 Vр-р	N/A
	Active mode	1 Vp-p with ±0.2 V offset	N/A
	Direct DAC mode	N/A	1 Vp-p (0 volt offset)
Corrected passband flatness	±0.5 dB DC - 500 MH	Iz (with 1.25 GHz clock)	
Corrected passband group delay	±150 ps rms DC - 500) MHz (with 1.25 GHz clock)	
Reconstruction filters	500 MHz and 250 MH	Iz realized as 7-pole Cauer Che	bychev filters plus thru-line output
Pulse response	Rise time (10 to 90%)	: < 1 ns Fall time (10 to 90%): <	1 ns Amplitude: 0.5 V pk-pk

2 A sync clock cycle is clock/8

LXI Class A Certified

Power	
90 to 132 VAC, 50 to 60 Hz, or 195 to 267	VAC, 50 to 60 Hz (automatically selected), 90 watts maximum
Environmental	
Operating temperature	0 to +50 °C (meets IEC-60068-2-1 and IEC-60068-2-2)
Storage temperature	-20 to +70 °C (meets IEC-60068-2-1 and IEC-60068-2-2)
Relative humidity	10 to 90% at 40 °C, non-condensing
Altitude	0 to 2000 m above mean sea level
Shock and vibration	
Transportation shock	50 G peak trapezoidal [meets IEC-60068-2-27]
End use handling shock	75 G peak, 1/2 Sine (2-3 ms) [meets IEC-60068-2-27]
Operating random	5-500 Hz, 0.21 g RMS [meets IEC-60068-2-64]
Survival swept sine	5-500 Hz, 0.5 g [meets IEC-60068-2-6]
Survival random	5-500 Hz, 2.09 g RMS [meets IEC-60068-2-6]
Safety	
Designed for compliance to EN 61010-1 (2	001)
EMC	
Meets the conduction and radiated interfe	rence and immunity requirements of EN 61326-1.
Weight	
5.0 kg (11 lb)	
Security	
All user data stored in volatile memory	
Dimensions	
2U, 1/2 rack wide	8.8 H x 21.6 W x 44.7 D cm (3.5 H x 8.5 W x 17.6 D inches) (conforms to LXI standards)
ISO compliance	
This modular instrument is manufactured i commitment to quality.	n an ISO-9001 registered facility in concurrence with Keysight Technologies

Ordering Information

Figure 11. Keysight N8242A 10-bit arbitrary waveform generator LXI module

N8242A 10-bit arbitrary waveform generator with 8 MS memory per channel

Options	
N8242A-125	1.25 GS/s sample rate
N8242A-062	625 MS/s sample rate
N8242A-016	Waveform memory expansion to 16 MSa per channel
N8242A-300	Enabling software for 16-bit dynamic sequencing
N8242A-330	Direct digital synthesis software

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